WHAT IS CLAIMED IS:

1. A phase locked loop circuit using a fractional frequency divider, comprising:

a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator with a deviation, which is obtained by dividing the frequency of the output of said first voltage-controlled oscillator by a first fractional frequency divider and by comparing the frequency-divided output with a reference frequency, through a low-pass filter; and

a second fractional frequency divider for dividing the frequency of the output of said first PLL stage and for inputting the frequency-divided output as a reference frequency signal of a second PLL stage,

wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.

2. A phase locked loop circuit using a fractional frequency divider, according to Claim 1,

wherein said second PLL stage is constructed to control the output frequency of said second voltage-controlled oscillator with a deviation, which is obtained by dividing the frequency of the output of said second voltage-controlled oscillator by frequency divider and by comparing the frequency-divided output with the reference frequency, through

a low-pass filter.

3. A phase locked loop circuit using a fractional frequency divider, comprising:

a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator in accordance with a deviation, which is obtained by comparing the output of said first voltage-controlled oscillator with a reference frequency through a DDS; and

a second PLL stage for controlling the output frequency of said second voltage-controlled oscillator in accordance with a deviation, which is obtained by using the output of said first PLL stage as a reference frequency signal and by comparing the output of a second voltage-controlled oscillator divided in frequency by a fractional frequency divider, with said reference frequency signal,

wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.

4. A phase locked loop circuit using a fractional frequency divider, comprising:

a first PLL stage for controlling the output frequency of a first voltage-controlled oscillator with a deviation, which is obtained by dividing the frequency of the output of said first voltage-controlled oscillator by a first fractional

frequency divider and by comparing the frequency-divided output with a reference frequency; and

a second PLL stage for controlling the output frequency of said second voltage-controlled oscillator in accordance with a deviation, which is obtained by using the output of said first PLL stage as a reference frequency signal and by comparing the output of a second voltage-controlled oscillator through a DDS, with said reference frequency signal,

wherein the output signal of a second voltage-controlled oscillator of said second PLL stage is extracted.

5. A phase locked loop circuit using a fractional frequency divider, according to any of Claims 1 to 4, further comprising:

a band-pass filter inserted into the front stage of a phase comparator of said first PLL stage.